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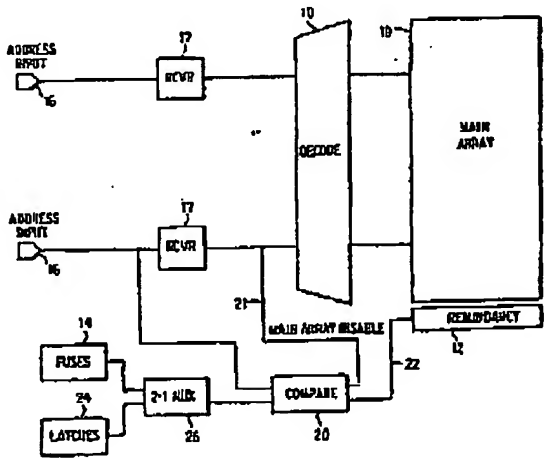
(54) Latch assisted fuse testing for customized integrated circuits.

(57) On-chip circuitry facilitates fuse testing in customized integrated circuits. The circuitry has specific application in testing fuse redundancy high end memories. A latch assisted fuse testing (LAFT) methodology employs an on-chip latch stack which can be used in place of the fuses. The latches in the stack are programmable and can perform the same function as the fuses during chip operation. This allows testing or experimentation to be performed nondestructively, without blowing any fuses. In one particular application of the invention, memory arrays with redundant blocks on a chip are provided with the on-chip latch stack. After the tests based on previously generated error data are performed using the latch stack, fuses are blown to repair the memory array by replacing defective memory blocks with redundant blocks.

FIG. 1



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EUROPEAN SEARCH REPORT

Application Number
EP 92 48 0103

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	EP-A-0 327 861 (SIEMENS) * the whole document *	1,4,6	G06F11/20
A	FR-A-2 611 401 (THOMSON SEMICONDUCTEURS) * the whole document *	1,2,4,6,7	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

G06F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	14 APRIL 1993	MASCHE C.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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E : earlier patent document, but published on, or after the filing date
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